**APPENDIX C**

ARM® Cortex™-A9 MPCore™ Full Specification

* 800 MHz dual-core processor supporting symmetric and asymmetric multiprocessing
* Each processor includes the following:
  + High-efficiency, dual-issue superscalar pipeline (2.5 MIPS\* per MHz)
  + NEONTM media processing engine for media and signal processing acceleration
  + Single- and double-precision floating-point unit
  + 32 KB instruction and 32 KB data caches
  + Cache coherence for enhanced inter-processor communication
  + Memory Management Unit with TrustZone® security technology
  + Thumb®-2 technology for enhanced code density, performance, and power efficiency
  + Jazelle® architecture extensions for accelerating Java Virtual Machine
  + Program Trace Macrocell for full visibility of processor instruction flow
* Shared 512 KB, 8-way associative L2 cache, lockable by way, line, or master
* Acceleration coherency port that extends coherent memory access beyond the CPUs
* Generic interrupt controller
* 32 bit general purpose timer
* Watchdog timer
* Available in Altera® Arria® V SoCs and Cyclone® V SoCs